

VERSION HISTORY

Index:

Page1	01	VERSION HISTORY
Page2	02	BLOCK DIAGRAM
Page3	03	POWER TREE
Page4	04	A733Core
Page5	05	GPIO ASSIGNMENT
Page6	06	A733 SYS
Page7	07	POWER AXP318 LPDDR5
Page8	08	UFS
Page9	09	LPDDR5 32X1
Page10	10	A733 Analog&High-speed
Page11	11	A733 GPIO
Page12	12	WIFI/BT AW869

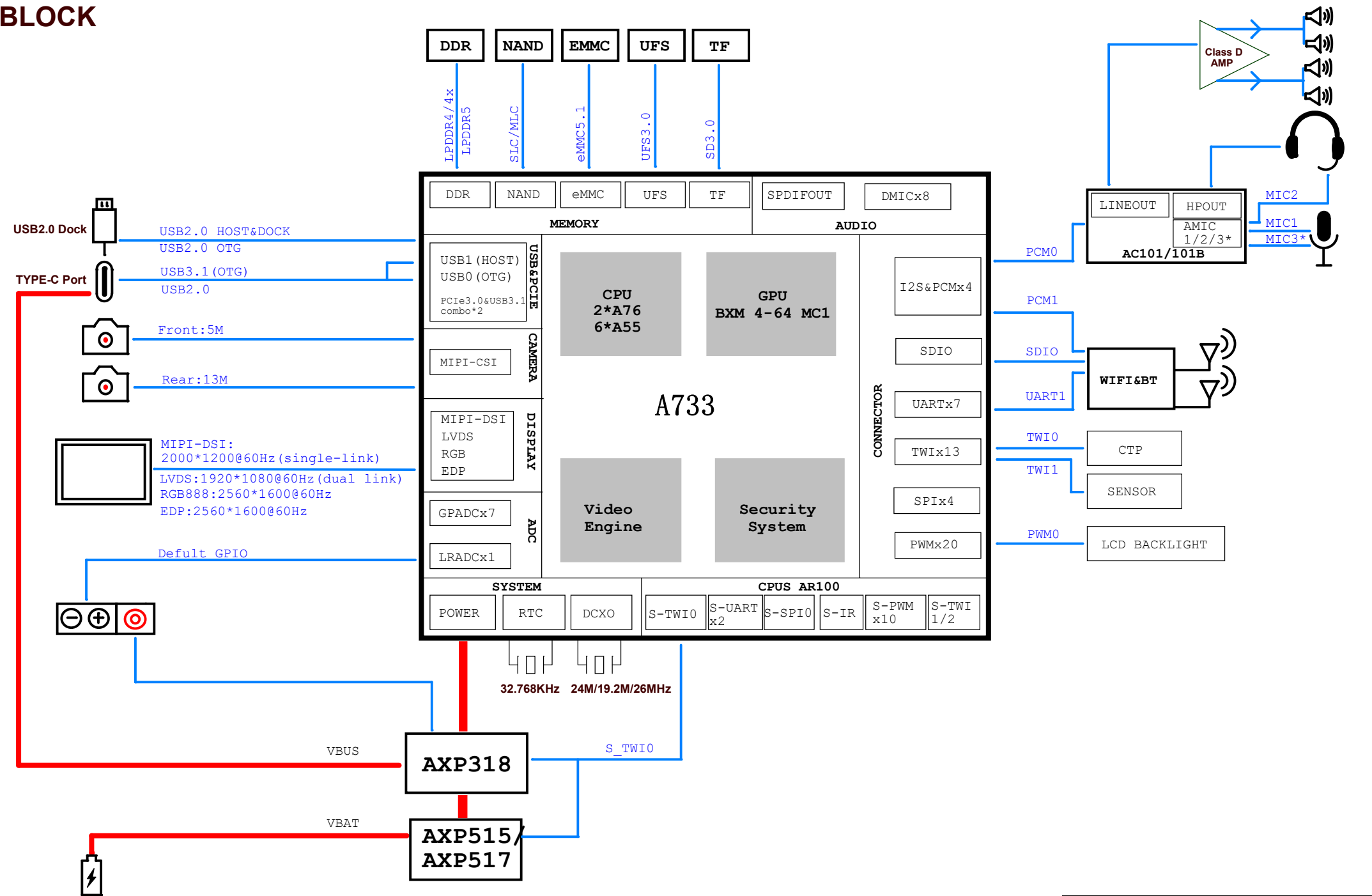
Revision	Description	Date
Ver 1.2	Release version	2025-09-19
Ver 1.4	1 添加4个Mark点.Add 4 Mark points. 2 PC0,PC1,PC5,PC6,PC8,PC9,PC10,PC11引脚接地.The pins PC0, PC1, PC5, PC6, PC8, PC9, PC10, and PC11 are grounded. 3 添加管脚COMB0-REF-CLKN, MB0-REF-CLKP。Add pins COMB0-REF-CLKN and MB0-REF-CLKP.	2025-11-19
Ver 1.5	1 移除管脚COMB0-REF-CLKN, MB0-REF-CLKP。并且接地。Remove pins COMB0-REF-CLKN and MB0-REF-CLKP.And be grounded.	

Description

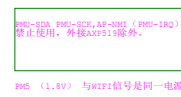
Note

Option

BLOCK







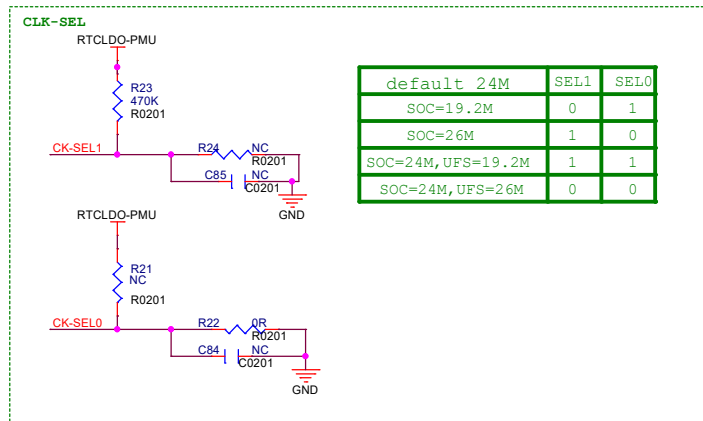
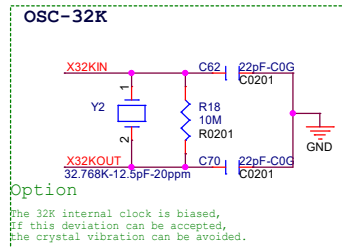
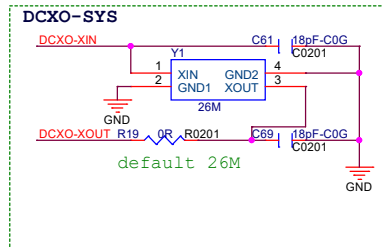
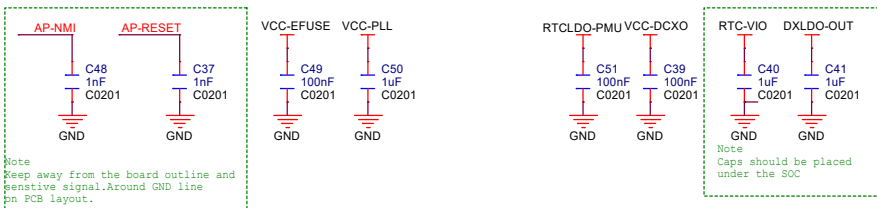
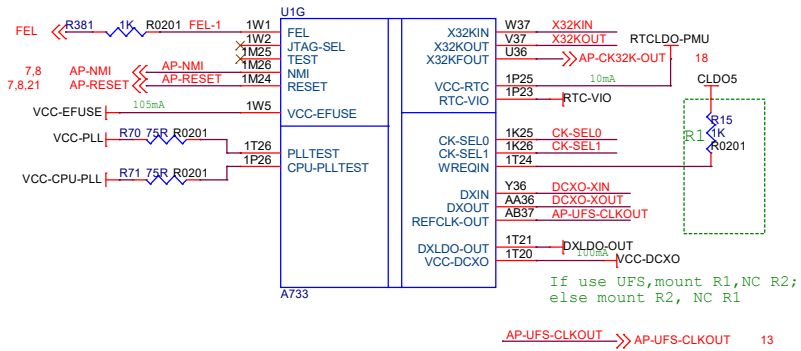
GPIO ASSIGNMENT

GPIO	Default	Function1
PB0	PB0	JTAG-MS
PB1	PB1	JTAG-CK
PB2	PB2	JTAG-DO
PB3	PB3	JTAG-DI
PB4	I2S0-MCLK	
PB5	I2S0-BCLK	
PB6	I2S0-LRCK	
PB7	I2S0-DOUT0	
PB8	I2S0-DIN0	
PB9	TWI0-SCK	UART0-TX
PB10	TWI0-SDA	UART0-RX
PC0	SDC2-DS	
PC1	SDC2-RST	
PC2		
PC3		
PC4		
PC5	SDC2-CLK	
PC6	SDC2-CMD	
PC7		
PC8	SDC2-D3	
PC9	SDC2-D4	
PC10	SDC2-D0	
PC11	SDC2-D5	
PC12		
PC13	SDC2-D1	
PC14	SDC2-D6	
PC15	SDC2-D2	
PC16	SDC2-D7	
PD0	DSIO-D0P	
PD1	DSIO-D0N	
PD2	DSIO-D1P	
PD3	DSIO-D1N	
PD4	DSIO-CKP	
PD5	DSIO-CKN	
PD6	DSIO-D2P	
PD7	DSIO-D2N	
PD8	DSIO-D3P	
PD9	DSIO-D3N	
PD10	SPI1-CS0	
PD11	SPI1-CLK	
PD12	SPI1-MOSI	
PD13	SPI1-MISO	
PD14	PD14	
PD15	SPI1-CS1	
PD16	TWI2-SCK	
PD17	TWI2-SDA	
PD18	PD17	
PD19	PD18	
PD20	PD19	
PD21	PD20	
PD22	PD21	
PD23	PWM0-5	

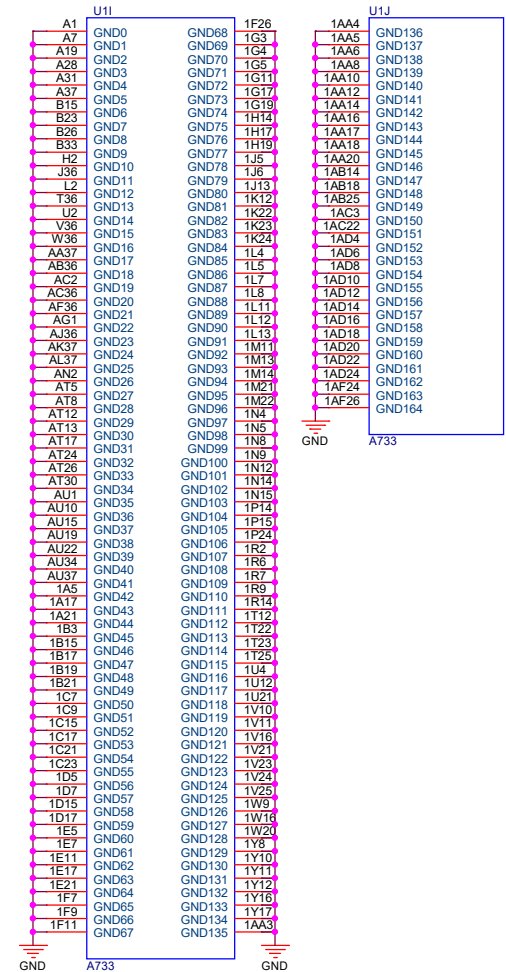
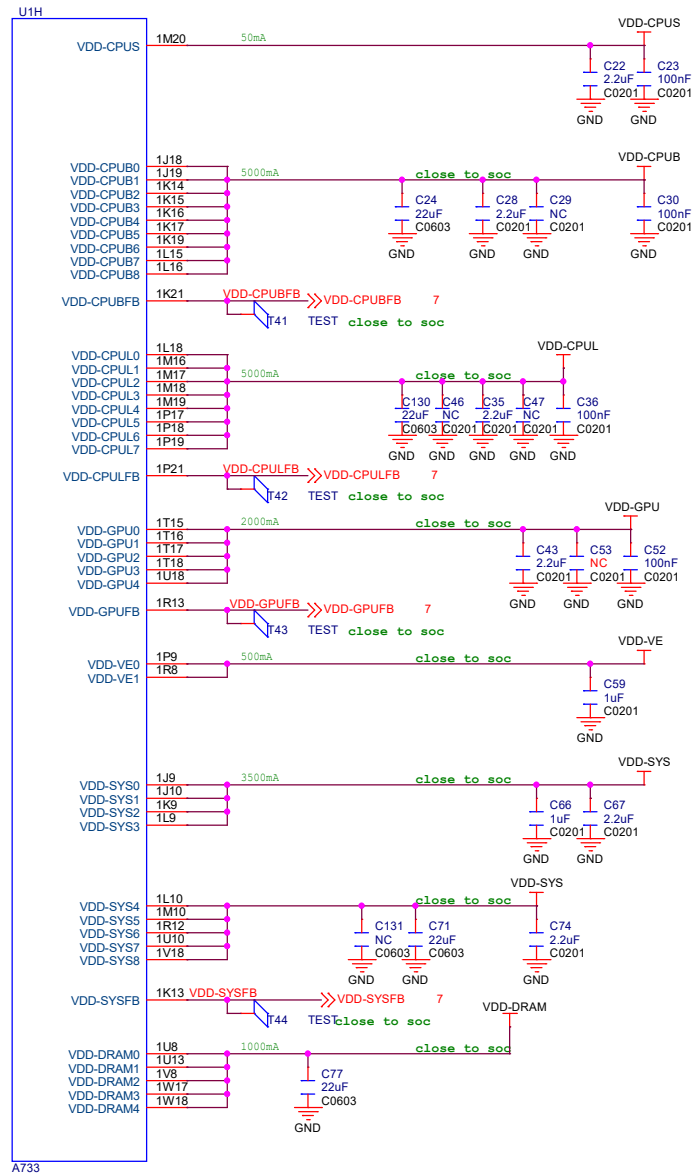
GPIO	Default	Function1
PE0		
PE1		
PE2		
PE3	TWI3-SCK	
PE4	TWI3-SDA	
PE5	MCSI1-MCLK	
PE6		
PE7		
PE8		
PE9		
PE10		
PE11		
PE12	PE14	
PE13	PE15	
PE14	PE16	
PE15	PE17	
PF0	SDC0-D1	
PF1	SDC0-CMD	
PF2	SDC0-CLK	
PF3	SDC0-D0	
PF4	SDC0-D3	
PF5	SDC0-D2	
PF6	SDC0-DET	
PG0	SDC1-CLK	
PG1	SDC1-CMD	
PG2	SDC1-D0	
PG3	SDC1-D1	
PG4	SDC1-D2	
PG5	SDC1-D3	
PG6	UART1-TX	
PG7	UART1-RX	
PG8	UART1-RTS	
PG9	UART1-CTS	
PG10		
PG11	I2S1-BCLK	
PG12	I2S1-LRCK	
PG13	I2S1-DOUT0	
PG14	I2S1-DIN0	
PH0		
PH1	PH1	
PH2	TWI1-SCK	
PH3	TWI1-SDA	
PH4	PH4	
PH5	PH5	
PH6	PH6	
PH7	PH7	
PH8	PH8	
PH9	PH9	
PH10	PH10	
PH11	PH11	
PH12		
PH13		
PH14	PH14	
PH15	BOARD-ID-SEL-GPIO	
PH16	DDR-PARA-SEL-GPIO	

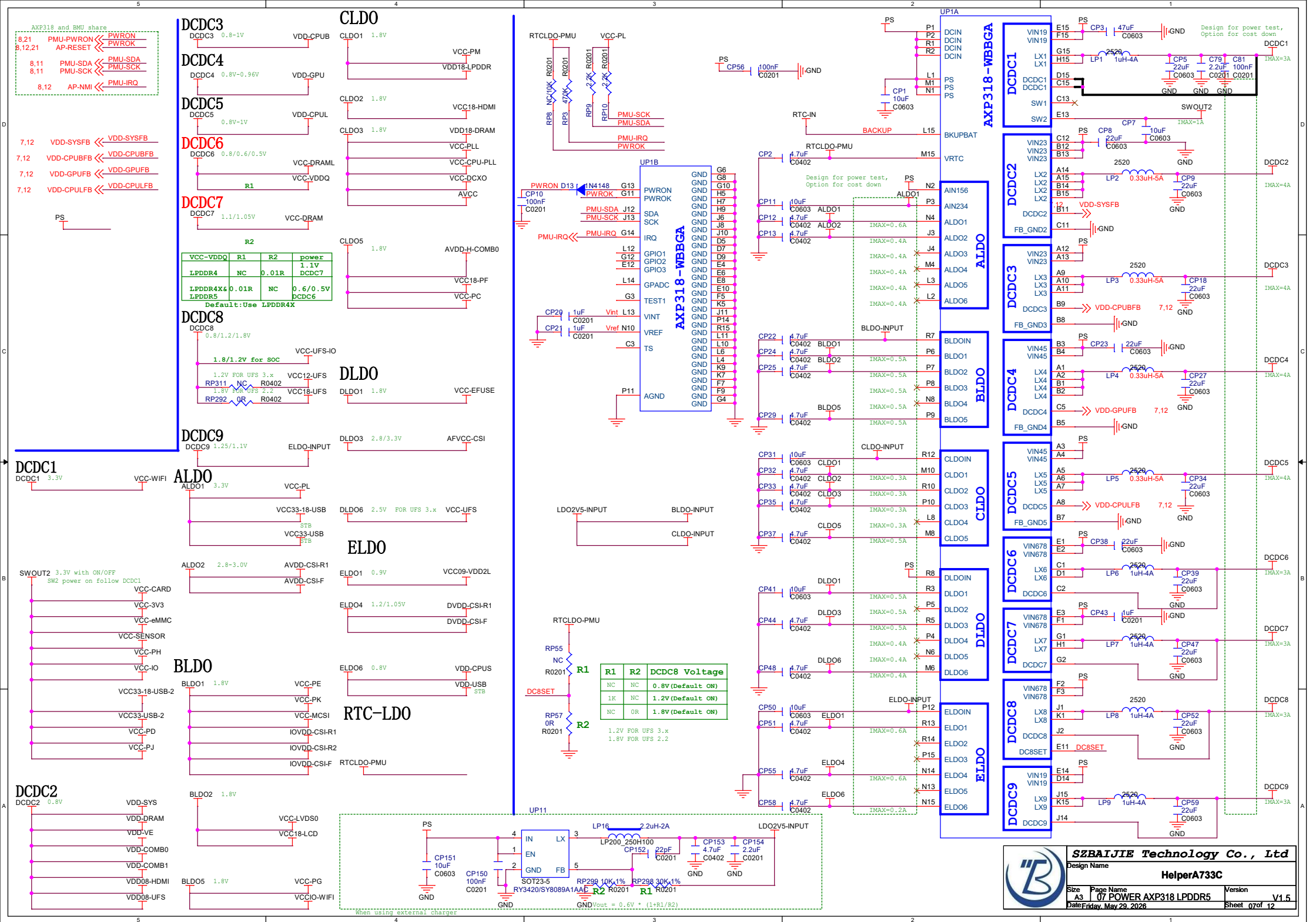
GPIO	Default	Function1
PJ22		
PJ23		
PJ24		
PJ25		
PJ26		
PJ27		
PK0		
PK1		
PK2		
PK3		
PK4		
PK5		
PK6		
PK7		
PK8		
PK9		
PK10	MCSIB-D0N	
PK11	MCSIB-D0P	
PK12	MCSIB-D1N	
PK13	MCSIB-D1P	
PK14	MCSIB-CKN	
PK15	MCSIB-CKP	
PK16	MCSIB-D2N	
PK17	MCSIB-D2P	
PK18	MCSIB-D3N	
PK19	MCSIB-D3P	
PK20	MCSIC-D0N	
PK21	MCSIC-D0P	
PK22	MCSIC-D1N	
PK23	MCSIC-D1P	
PK24	MCSIC-CKN	
PK25	MCSIC-CKP	
PL0	S-TWI0-SCK	
PL1	S-TWI0-SDA	
PL2	PL2	S-UART1-TX
PL3	PL3	S-UART1-RX
PL4	PL4	S-JTAG-MS
PL5	PL5	S-JTAG-CK
PL6	PL6	S-JTAG-DO
PL7	PL7	S-JTAG-DI
PL8	PL8	
PL9	PL9	
PL10		
PL11		
PL12		
PL13		
PM0	PM0	
PM1	PM1	
PM2	PM2	
PM3	PM3	
PM4	PM4	
PM5	PM5	

SYS

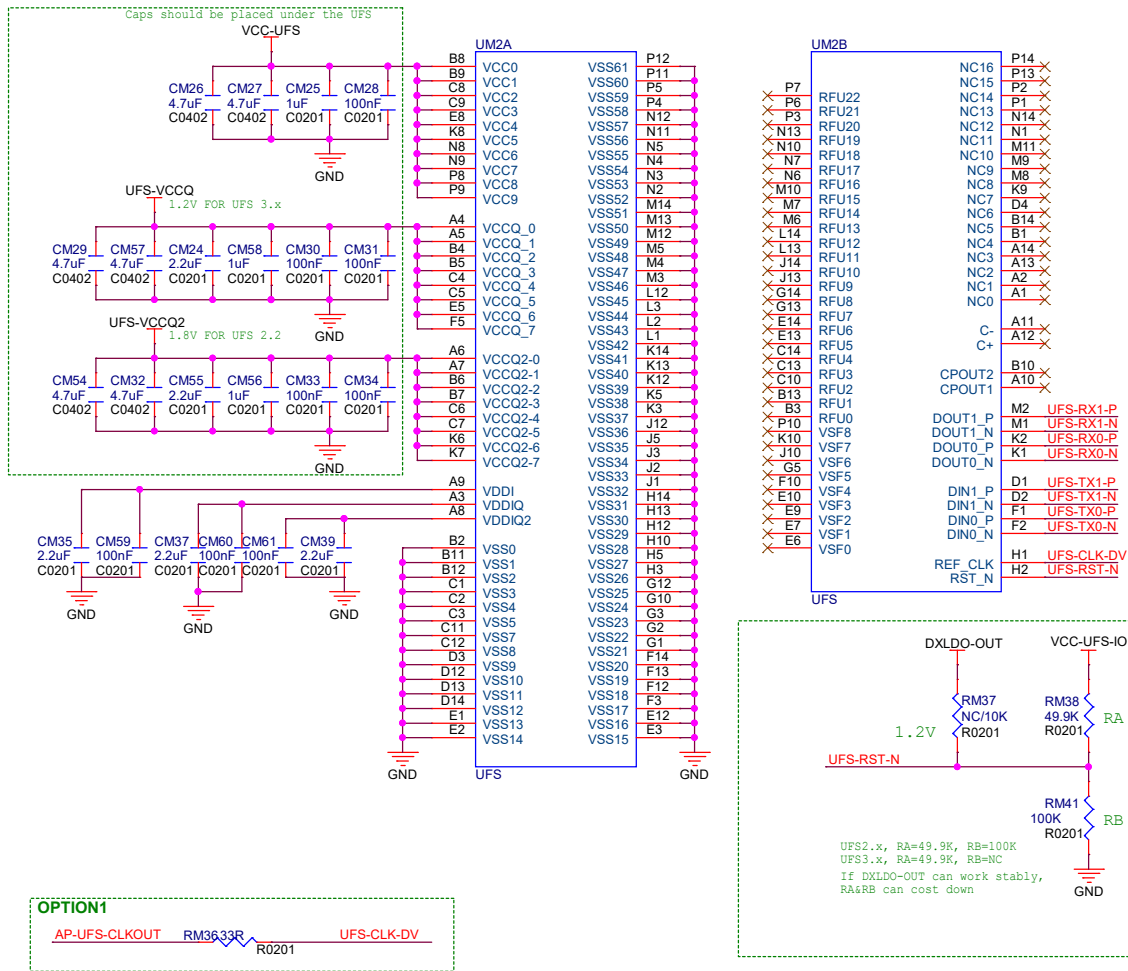
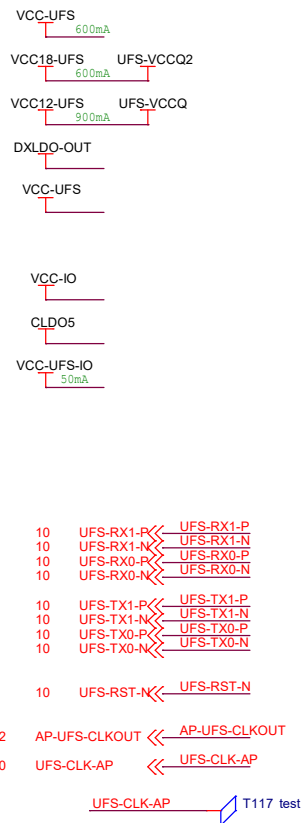


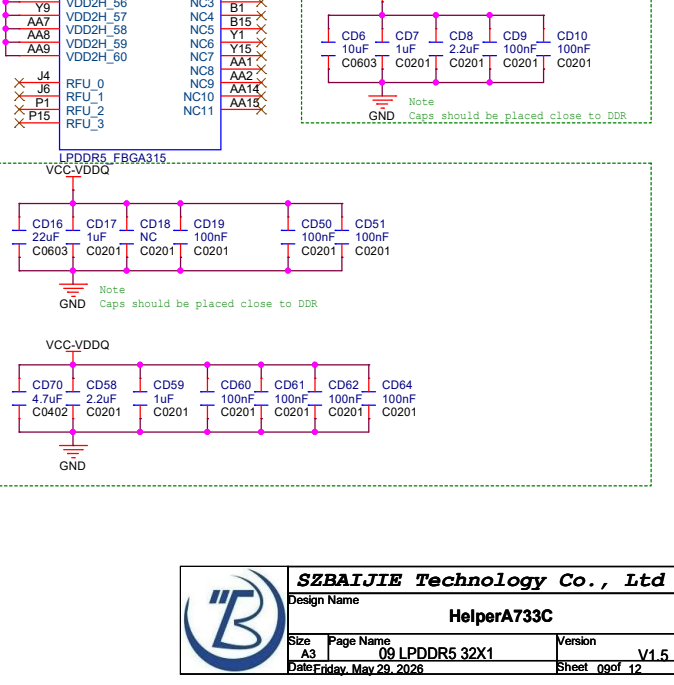
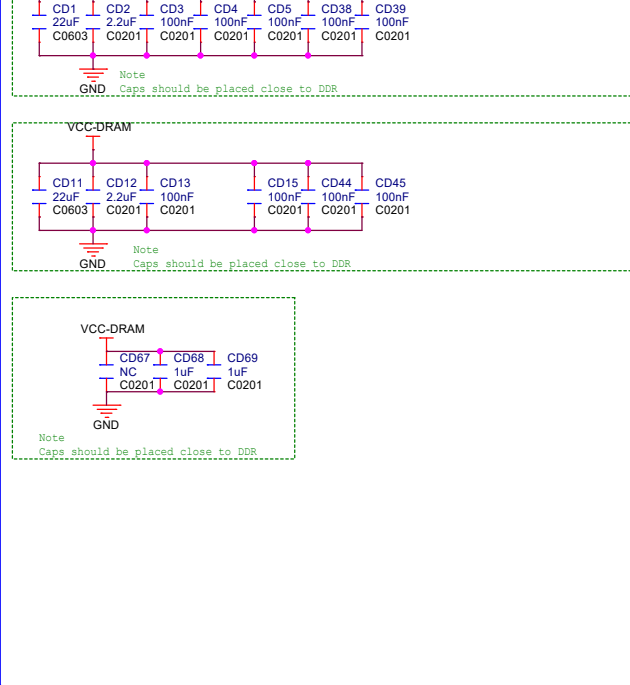
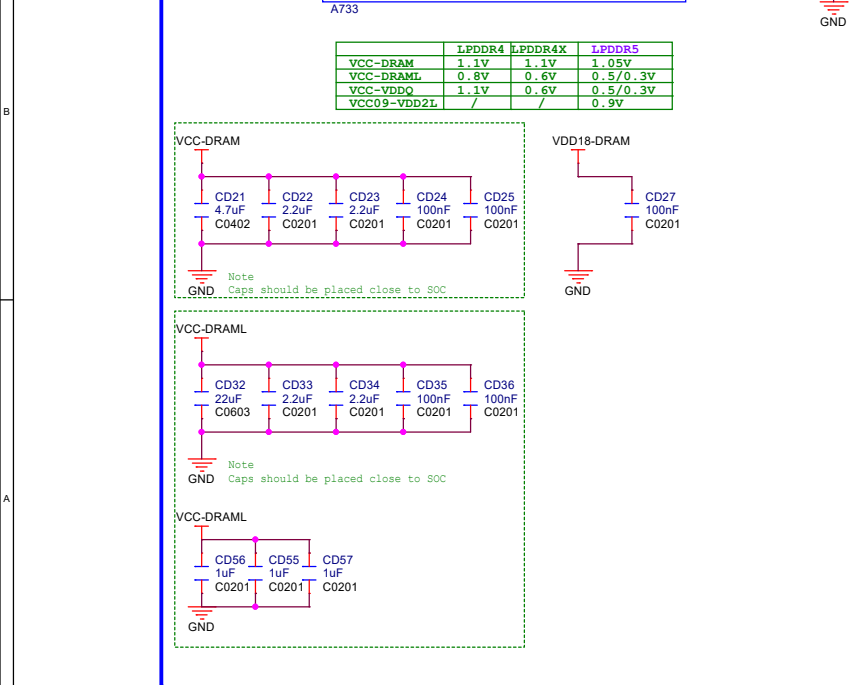
CORE POWER



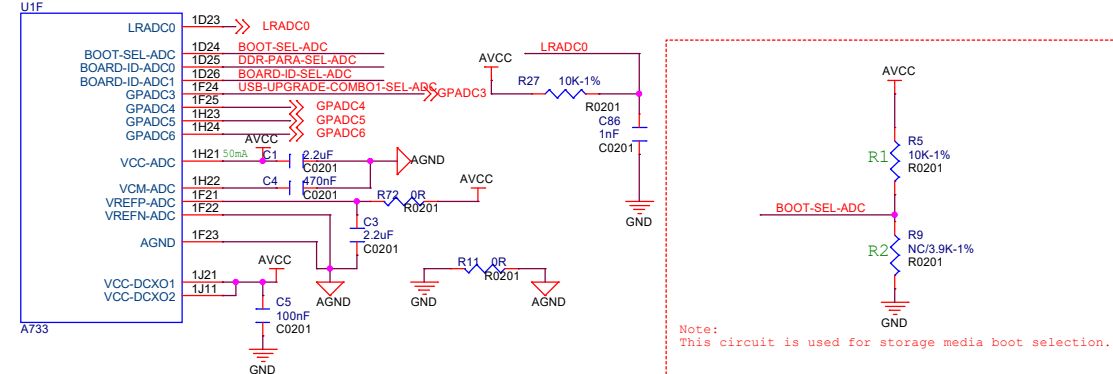


UFS

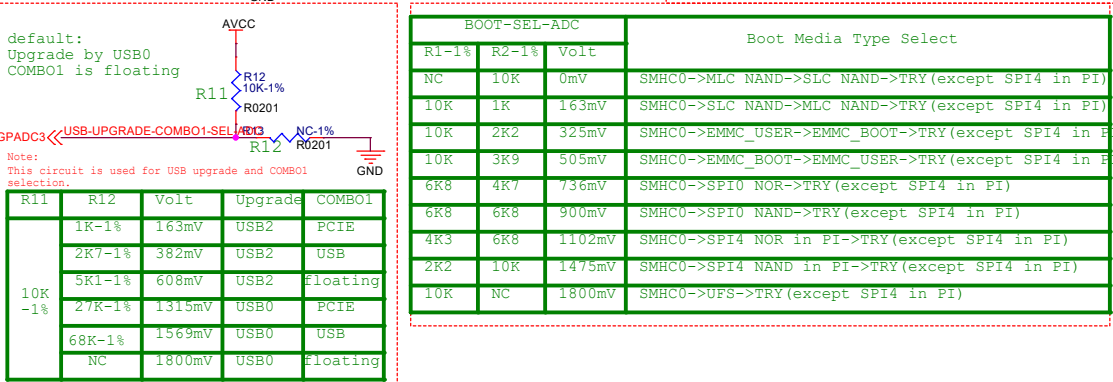




ADC



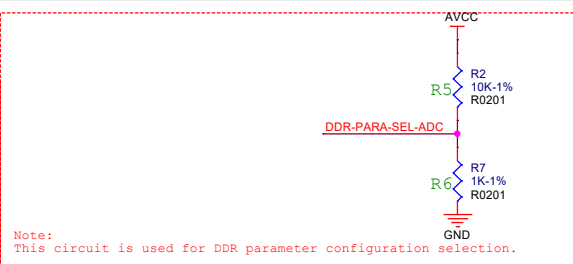
Note:
This circuit is used for storage media boot selection.



Note:
This circuit is used for USB upgrade and COMB01 selection

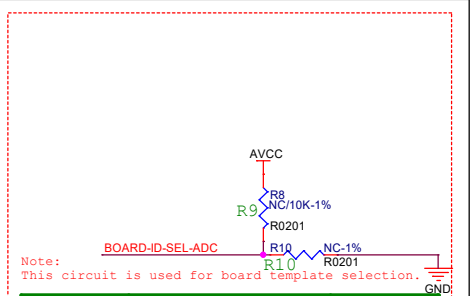
R11	R12	Volt	Upgrade	COMBO1
10K -1%	1K-1%	163mV	USB2	PCIE
	2K7-1%	382mV	USB2	USB
	5K1-1%	608mV	USB2	floating
	27K-1%	1315mV	USB0	PCIE
	68K-1%	1569mV	USB0	USB
	NC	1800mV	USB0	floating

BOOT-SEL-ADC			Boot Media Type Select
R1-1%	R2-1%	Volt	
NC	10K	0mV	SMHC0->MLC NAND->SLC NAND->TRY(except SPI4 in PI)
10K	1K	163mV	SMHC0->SLC NAND->MLC NAND->TRY(except SPI4 in PI)
10K	2K2	325mV	SMHC0->EMMC_USER->EMMC_BOOT->TRY(except SPI4 in PI)
10K	3K9	505mV	SMHC0->EMMC_BOOT->EMMC_USER->TRY(except SPI4 in PI)
6K8	4K7	736mV	SMHC0->SPI0 NAND->TRY(except SPI4 in PI)
6K8	6K8	900mV	SMHC0->SPI0 NAND->TRY(except SPI4 in PI)
4K3	6K8	1102mV	SMHC0->SPI4 NOR in PI->TRY(except SPI4 in PI)
2K2	10K	1475mV	SMHC0->SPI4 NAND in PI->TRY(except SPI4 in PI)
10K	NC	1800mV	SMHC0->UFS->TRY(except SPI4 in PI)



Note: This circuit is used for DDR parameter configuration selection.

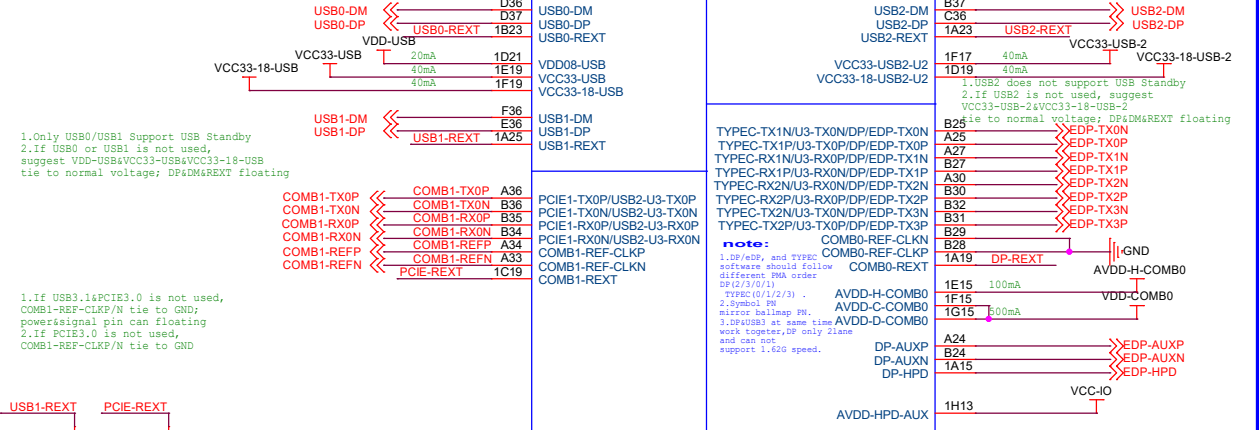
GPIO Level(Set by the R3 pull-up and R4 pull-down resistance of PH16 GPIO)	GPADC Voltage(Fixed pull-up R5 is 10K-1 Ω ,Set the voltage by adjusting pull-down resistor R6)	DDR PARA
0	163mV (1K-1 Ω)	DDR PARA 0
0	382mV (2.7K-1 Ω)	DDR PARA 1
0	608mV (5.1K-1 Ω)	DDR PARA 2
0	811mV (8.2K-1 Ω)	DDR PARA 3
0	1050mV (14K-1 Ω)	DDR PARA 4
0	1315mV (27K-1 Ω)	DDR PARA 5
0	1569mV (68K-1 Ω)	DDR PARA 6
0	1800mV (NC)	DDR PARA 7
1	163mV (1K-1 Ω)	DDR PARA 8
1	382mV (2.7K-1 Ω)	DDR PARA 9
1	608mV (5.1K-1 Ω)	DDR PARA 10
1	811mV (8.2K-1 Ω)	DDR PARA 11
1	1050mV (14K-1 Ω)	DDR PARA 12
1	1315mV (27K-1 Ω)	DDR PARA 13
1	1569mV (68K-1 Ω)	DDR PARA 14
1	1800mV (NC)	DDR PARA 15



Note:
This circuit is used for board template selection.

GPIO-SET		BOARD-ID-SEL-ADC			BoardID Config
R7	R8	R9	R10	Volt	
NC	1K pull down	10K -1%	1K-1%	163mV	Config-1
			2K7-1%	382mV	Config-2
			5K1-1%	608mV	Config-3
			8K2-1%	811mV	Config-4
			14K-1%	1050mV	Config-5
			27K-1%	1315mV	Config-6
			68K-1%	1569mV	Config-7
			NC	1800mV	Config-8
47K pull up	NC	10K -1%	1K-1%	163mV	Config-9
			2K7-1%	382mV	Config-10
			5K1-1%	608mV	Config-11
			8K2-1%	811mV	Config-12
			14K-1%	1050mV	Config-13
			27K-1%	1315mV	Config-14
			68K-1%	1569mV	Config-15
			NC	1800mV	Config-16

USB&EDP&PCIE



Only USB0/USB1 Support USB Standby, USB2 does not support USB Standby
 combo1 (USB3.1 1lane/PCIE3.0 1lane), combo0 (DP1.4 4lane/DP1.4 2lane+USB3.1 1lane)

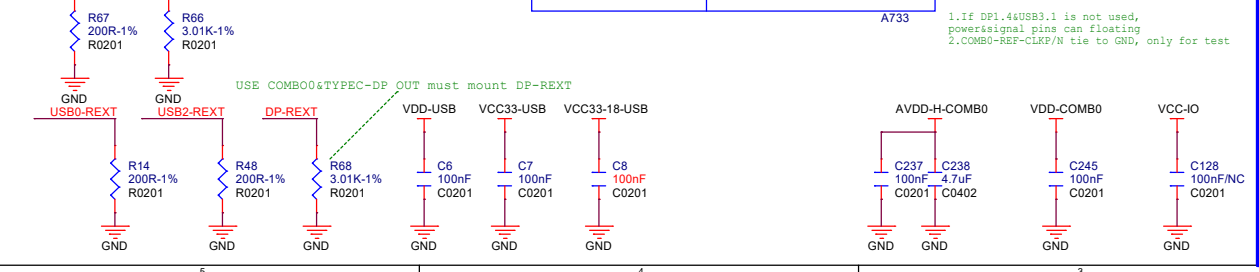
1.Only USB0/USB1 Support USB Standby
2.If USB0 or USB1 is not used,
suggest VDD-USB&VCC33-USB&VCC33-18-USB
tie to normal voltage; DP&DM&REXT floating

1.If USB3.1&PCIE3.0 is not used,
COMB1-REF-CLKP/N tie to GND;
power&signal pin can floating
2.If PCIE3.0 is not used,
COMB1-REF-CLKP/N tie to GND

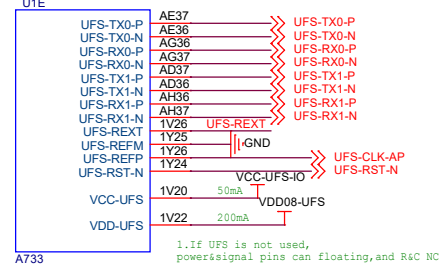
note:

- 1.DP/eDP, and TYPEC software should follow different PMA order DP(2/3/0/1)
2. TYPEC(0/1/2/3) .
- 2.Symbol FN mirror ballmap FN.
- 3.DP4USB3 at same time work together,DP only 2lane and can not support 1.62G speed.

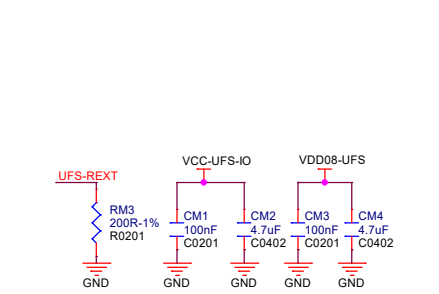
- 1.If DP1.4&USB3.1 is not used, power&signal pins can floating
- 2.COMB0-REF-CLKP/N tie to GND, only for test



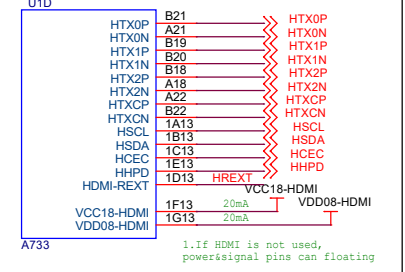
UFS



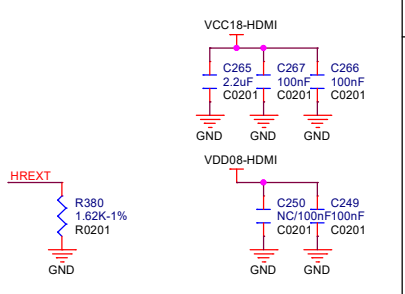
1.If UFS is not used,
power&signal pins can floating,and R&C NC



HDMI



1.If HDMI is not used,
power&signal pins can floating



GPIO



AW869A

